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Implementation of D-flipflop using Hybrid Memristor with CMOS Transistor

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Abstract

The preamble of the memristor has covered the mode to various inventions. The memristor has a characteristic of non-volatility and it is the nano-scale element which replaces the CMOS transistor. In this work, the sequential element designed with Hybrid CMOS/Memristor technology. The D-flipflop is designed using the memristor with CMOS transistor. Its feature is non-volatile and it performs the analysis is compared with different D-flipflop designs. The proposed D-flipflop is designed with hybrid memristor and CMOS transistors using 90nm technology in cadence virtuoso tool. The simulations are carried out using spectre. The power and delay of the proposed circuit are reduced when compared with existing design and energy consumption is also decreased.

Keywords

Sequential Element, D-Latch, Memristor, Nonvolatile, CMOS Technology.

Introduction

The possible way of Moore's law extends beyond the limitations of scaling of the transistor is to acquire the equivalent functionality of the circuit using fewer elements or components [1]. The circuits of the CMOS transistors and implementation of Boolean logic beyond the 10nm limit are at greatest hesitant. The key explanation is to facilitate that length of the gate beyond 10nm, the MOSFET parameter sensitivity is to be predictable [2]. Currently, in the research of the VLSI, the engineers are insinuating for better electrical property component which is used for logic blocks. In this paper, a new nano-scale device known as memristor is introduced and it represents from Memory resistor for the reason that, it can memorize the charge flown through it by varying its resistance [3]. This memristor has a better packing density, low sustaining voltage, high switching speed, and non- volatility [4-5]. Fig.1 shows the Memristor model, and Voltage versus Current characteristics with the frequency of 60MHz.

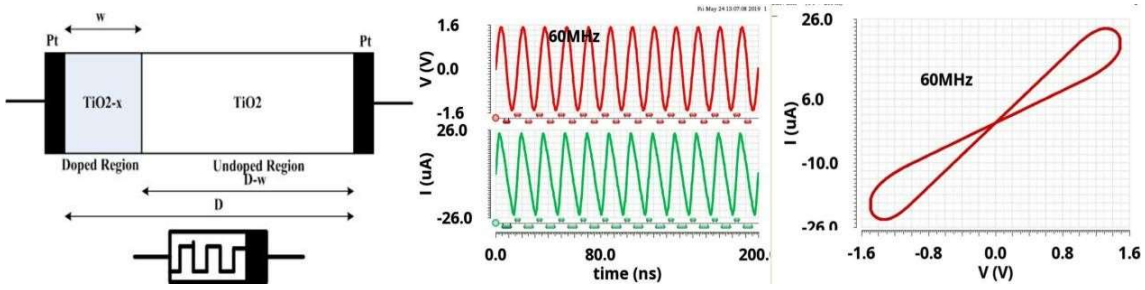

Fig. 1: Memristor Symbol, Input and Waveforms with Frequency of 60MHz, V-I Characteristics of Memristor

This Memristor model is developed by Leon Chua in 1971 [6-7], further, it develops in HP laboratories in 2008. Normally, a time-invariant voltage-controlled Memristive device is indicated by [8].

$$v = M(t).i \quad (1)$$

$$M = \frac{d\emptyset}{dx} \quad (2)$$

$$\frac{dx(t)}{dt} = f(x,i) \quad (3)$$

where *v* stands for voltage across the memristor, *i* demonstrates current throughout the memristor, *M(t)* identifies Memristance and *x(t)* refers to memristor's internal state. The VTEAM model illustrates [9],

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$$M(t) = R_{ON}\left(\frac{w(t)}{D}\right) + R_{OFF}\left(1 - \frac{w(t)}{D}\right) \quad (4)$$

$$\frac{dx(t)}{dt} = k.i(t) \quad (5)$$

$$x(t) = \frac{w(t)}{D} \in (0,1) \quad (6)$$

$$k = \frac{\mu_v R_{ON}}{D^2} \quad (7)$$

where w(t) specifies doped region width, D named as length, R_{ON} and R_{OFF} characterize the resistance of low and high value, and the constant μ_V exemplifies oxygen vacancies average mobility.

The basic building blocks of sequential circuits are Flip flops which are used to store single bit binary information either 0 or 1. The functionality of flip flops can be defined by set, reset, flip, and hold. These are working on the basis of the input signal and clock signal, accordingly broad usage of digital sequence in the generation, transformation, and storage. A D-flop flop is used more frequently in sequential circuits rather than other flip-flops. This D flip flop is shown in Fig. 2. When the clock is high, the output follows input, and which has the same value of the input. On the other, the clock is low, the output Q and Q_bar maintain the same despite the altering of the input [10]. Section II describes the proposed D-flipflop, section III explains the simulation results of D-flip flop, and section IV justifies the conclusion of this work.

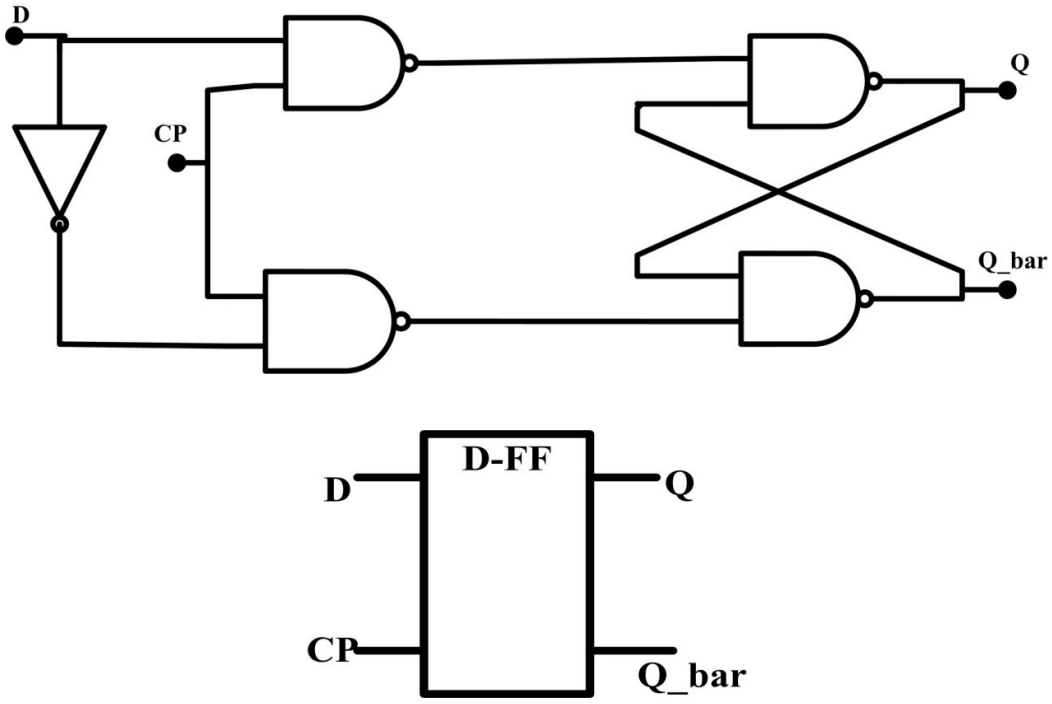

Fig.2: D-flipflop

Proposed D-flipflop

The proposed D-flip-flop in this work is shown in Fig.3 uses 11 transistors (6 transistors in OR Logic gate) and 4 Memristors. The functionality of D flip-flop is selected by the reading (READ) and writing (CLK) procedure of the OR gate functionality. The D-flip-flop operation is discussed in four ways. (1)Flip-flop circuit (2)Holding of logic information (3)Resistive switching (4)Usual operation.

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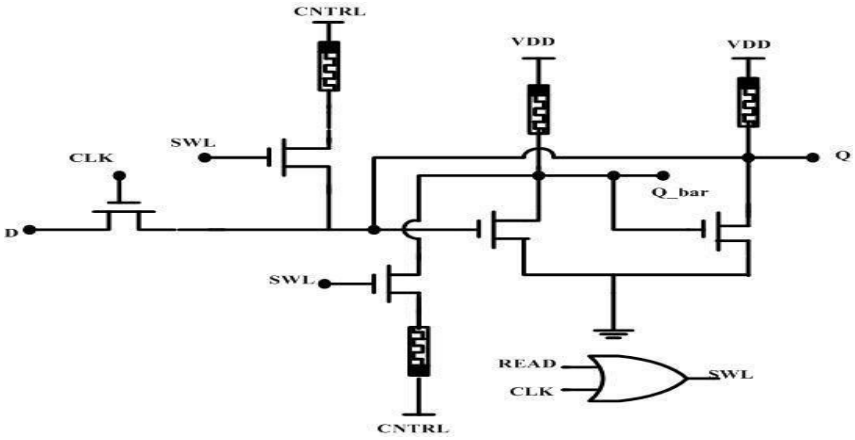

Fig. 3: Proposed D-Flip flop

Flip-flop Circuit

The clock(CLK) and D are the inputs and Q and Q_bar are the outputs of the flip flop. The operation of the circuit depends on the clock (CLK). When the CLK has low value, the pass transistor becomes in non-conducting region, hence there is no path amid the input and output. Consequently, the output does not depend on the input. On the other, when the CLK has high value, the pass transistor becomes in conducting region, hence there is a path between the input and output. Thus, output depends on input and output acquires the same as the input. Thus, the circuit acts as a flip flop.

Holding of Logic Information

The two inverters containing CMOS transistor and Memristor connected end to end is utilized for storing information of logic values which are considered as temporary usages. One inverter output connected to the input of another inverter and vice versa. This implementation gives complementary logic. This ensures that power supply is not disturbed for inverters which provide that the output is not altered for the low value of CLK.

Resistive Switching

The programming and retrieving storage logic information can be examined by the Memristors and which is controlled by the SWL depends on CLK and READ. The conducting path is activated in between outputs(Q and Q_bar) and Memristors when the CLK has a high value. This permits the flow of current between outputs and CNTRL through the memristors and vice versa. This exhibits bidirectional flow of currents through the memristors which made the memristors to maintain states or switching operation. This CNTRL switch is fixed to 0.6 V(constant voltage).

If the input D and CLK is high, the output Q is at high and Q_bar is low. At that moment, the pass transistor SWL is in conducting region makes a Memristor corresponding to Q switched to Resistance state of Low value and a Memristor corresponding to Q_bar switched to Resistance state of High value. Equally, if the D input is low and CLK is high, the output Q is at low and Q_bar is high. At that moment, the pass transistor SWL is in conducting region makes a Memristor corresponding to Q switched to Resistance state of High value and a Memristor corresponding to Q_bar switched to Resistance state of Low value. If the CLK is low, The SWL produces a path of High resistance value amid Memristors and outputs.

Usual Operation

The low value of SWL is obtained when CLK and READ signals are low. The corresponding memristors connected to SWL through the transistors conserve their states due to the NMOS transistors are in non-conducting region. The flow of current is stopped between the Memristors and outputs(Q and Q_bar) because of non conducting transistors, hence no path between the CNTRL and output. Thus, the states of the Memristor are retained. As a result, the loss of flip flop's logic information has not occurred. The proposed D-flip flop functionality is summarized in Table 1.

Table 1: Brief Information of the Usual Operation

Clock	Read	D	Q	Q_bar
Low	x	x	Previous Q	Previous Q_bar
High	x	Low	Low	High
High	x	High	High	Low

Simulation Results of D-flipflop

The proposed design is carried out using Cadence virtuoso tool and simulation results are done using Spectre. This is shown in Fig. 4. The proposed design has power dissipation reduced to 60.38% and its value is 1.370μW. The

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delay is reduced to the value of 28.79ps. The energy consumption is reduced to the value of 292.9pJ. The comparison results of different D-flipflops are defined in Table 2.

Table 2: Comparison of Parameters of Different D-flip flops

Design	Power(W)	Delay(s)	Energy(J)
Conventional D-Flip flop of memristor [3]	97.50 µ	195.8p	16.71n
D-Flip flop using Memristor [11]	2.2686 µ	200 µ	499.2p
Proposed D-Flip Flop	1.370 µ	28.79p	292.9p

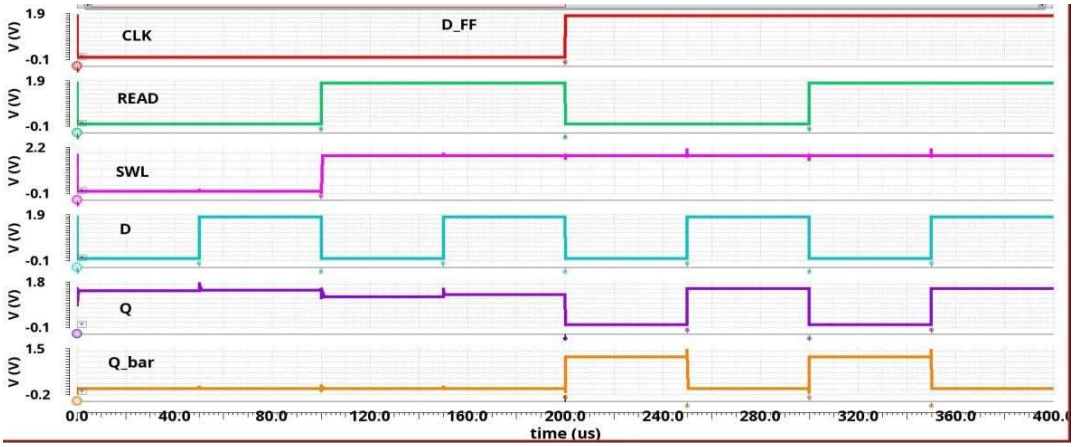

Fig. 4: Simulation Results of Proposed D-Flip flop

Conclusion

The proposed D-flip flop is summarized in this work. The D-flip flop is designed using CMOS transistors with Memristor and it is compared with traditional D-flip flop. The parameters like power dissipation, delay, and energy consumption are analyzed when compared with conventional D-flip flop. Finally, the non-volatile D flip flop design is summarized with the reduction of power dissipation, delay, and energy consumption.

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