

---

## Line Synchronised Control Pulses for Three Phase Induction Motor AC-AC Drive Using Analog Phase Lock Loop Technique

---

<sup>\*1</sup>Sangita H Deshmukh, <sup>2</sup>Vinay T Barhate, <sup>3</sup>Dhananjay R Tutakne

<sup>1,2</sup> Shri Ramdeobaba College of Engineering and Management, Nagpur

<sup>3</sup>Wainganga College of Engineering, Nagpur

Email: [deshmukhsh@rknec.edu](mailto:deshmukhsh@rknec.edu), [barhatevt@rknec.edu](mailto:barhatevt@rknec.edu), [dhananjaydrt@rediffmail.com](mailto:dhananjaydrt@rediffmail.com)

Received: 20th November 2019, Accepted: 31st January 2020, Published: 29th February 2020

### Abstract

Technique used in this research is to obtain high operating efficiency of three phase induction motor (IM). To achieve this emphasis is given on minimizing the core losses by controlling the magnetizing current of three phase induction motor so that total power loss gets reduced and thereby efficiency of IM gets improved. Improvement in power factor of IM causes reduction in magnetizing current. Novel topology used in this work also aimed at controlling the speed and improvement of power factor separately. To improve the performance and to obtain the expected results of induction motor at any change in operating frequency, work is focused on obtaining line synchronised extinction angle ( $\beta$ ) and Pulse Width Modulation(PWM) control pulses. Both these controls are line synchronized using analog phase lock loop(PLL) technique so that switching frequency of PWM pulses remains synchronized with the supply frequency for any small change in input supply frequency, so that separate smooth control over wide range of speed and improvement in power factor both are achieved. Switching off supply at extinction angle  $\beta$  gives improvement in power factor and variation in duty ratio of PWM pulses controls the speed of three phase induction motor. Hardware and simulation results are obtained by using only four switches, which simplifies the circuit and makes it cost effective. The hardware model for line synchronised control pulses using analog PLL technique is shown. PLL has many applications.

### Keywords

Extinction Angle ( $\beta$ ), Power Factor (PF), Induction Motor (IM), Phase Lock Loop (PLL), Pulse Width Modulation (PWM)

### Introduction

This paper presents phase lock loop analog (PLL) technique[10] to synchronize extinction angle and switching frequency of pulse width modulation pulses with the input supply voltage frequency. In PLL circuit phase of an output signal is related to the phase of an input signal. It is a closed loop system. In this work analog PLL circuit is designed by assembling a phase detector (PD) circuit, low pass filter (LPF) and voltage controlled oscillator (VCO). PD and LPF are the forward path functions whereas VCO is in feedback loop of the circuit. [3] [6] [7] [9] The function of phase detector is to compare the phase of the periodic signal generated by the oscillator with the phase of the input periodic signal and to adjust the oscillator so that the phases of both the signals are matched. In this work for controlling speed of IM, PWM technique with variable duty ratio at high switching frequency is used. For synchronisation of pulses switching frequency must be the multiple of the input supply frequency, which is perfectly obtained by using PLL technique. Variable extinction angle control technique is used to obtain high power factor of motor on wide range of speed with the variation in load. Both these pulses i.e. PWM and extinction angle control pulse are added together and synchronized with the input supply frequency using PLL technique so that any small variation in the supply frequency, will not cause any malfunction of three phase AC-AC induction motor drive. Additional circuitry of PLL may increase the cost of drive but since both the control pulses are added together, synchronization of these pulses simultaneously becomes the need of this drive. Thus unique technique has been used for control pulses. In this work it has been observed that improvement in power factor, reduces the motor current. And novel feature of the proposed topology is that, torque component of the input current increases and magnetizing component of current decreases, therefore overall current intake of the motor is reduced, which will result in reduced power consumption. [1] Since the magnetizing component of current is reduced stator copper loss ( $I^2R$ ) of the motor is also reduced. This defiantly improves the efficiency of the motor. Vector control technique and in (direct torque control) DTC control technique is also aimed at increasing the torque component of current and decreasing the magnetizing component of the current. In proposed research work it has been achieved and realized by using novel topology of line synchronized control pulses at variable switching frequency.

### Research Methodology and Line Synchronized Control Pulses:

Since without drive, three phase induction motor current lags with respect to the motor voltage by an angle  $\theta$ . To minimize phase angle  $\theta$ , supply voltage is cut off at an extinction angle  $\beta$ . Switching off the motor supply at

an angle  $\beta$ , makes the fundamental component of motor current to drag ahead the motor voltage which in turn results in minimizing the value of phase angle  $\theta$ , and thus power factor of IM gets improved.

The relation between  $\theta$  and  $\beta$  is given as,  $\cos(\theta) = \cos(\frac{\beta}{2}) \cos(\theta) = \cos(\frac{\beta}{2})$

$\cos(\theta) = \cos(\frac{\beta}{2})$  For optimum value of  $\beta$ , leading power factor can also be achieved. To obtain the variation in speed input supply is fed using PWM with variable duty ratio up to angle  $\beta$  only. Fig 1 represents the waveforms of methodology used in this work. As shown in figure 1 motor current (green color waveform) is lagging w.r.t. Line voltage (blue color waveform) by an angle  $\theta$ . If motor supply is stopped at an extinction angle ( $\beta$ ) then fundamental component of motor (red color waveform) current is dragged by an amount  $\beta/2$ . PWM pulses (black color waveform) are obtained till extinction angle  $\beta$  only. Figure. 2 represents the addition of PWM and extinction angle control pulse over a period of 180 degree. For three phases R,Y and B ,pulses are phase shifted by an angle 120 degree. Figure 3 represents simulation of the methodology for two different extinction angle which shows that Fundamental component of load current is leading w.r.t. supply voltage (motor voltage) of phase A

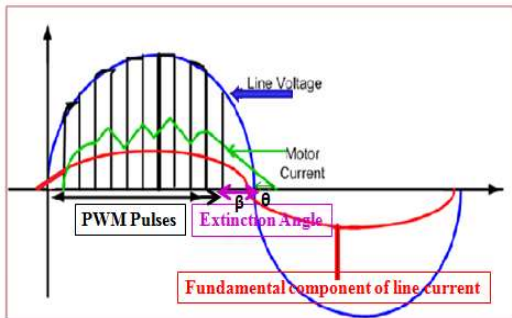


Fig 1 : Research Methodology Used in Work

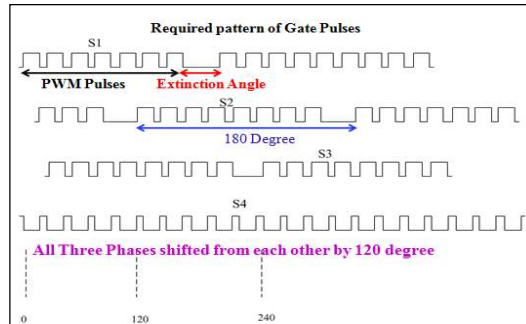


Fig 2: Addition of PWM and Extinction Angle Pulse for R,Y,B Phase

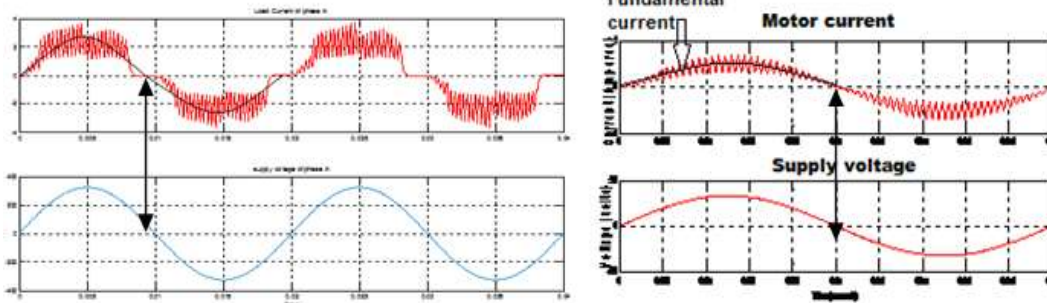
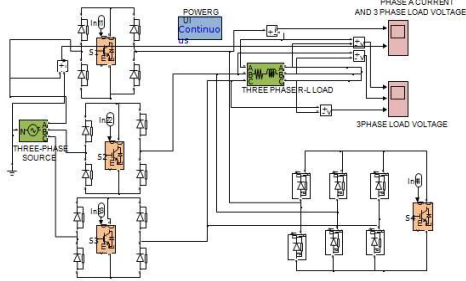


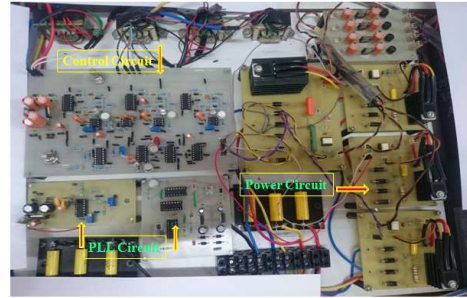
Fig 3: Simulation of Methodology Indicating Fundamental Component of Load Current Leading w.r.t. Supply Voltage of Phase A

**Circuit Connection of Proposed Topology:**

Figure 4 represents simulation circuit which shows that three switches are connected in series with three phase windings and fourth switch known as freewheeling switch is connected across three phase winding through three phase diode rectifier bridge circuit so that three phase motor current can circulate through a single switch when motor supply is switched off at extinction angle  $\beta$ . [2] [4] [5] Figure 5 represents hardware circuit which consists of power circuit, control circuit and PLL circuit. Supply to control circuit is given through PLL circuit which keeps switching frequency of PWM pulses absolutely synchronised with the input supply frequency,



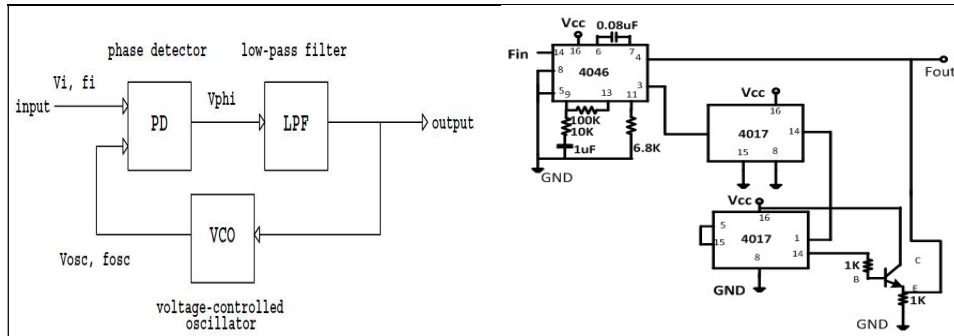
**Fig 4: Simulation Model of Proposed Scheme**



**Fig 5: Complete Hardware with PLL Circuit of Proposed Scheme**

**Line Synchronized PWM and Extinction Angle Control Pulses Using PLL Technique:**

Phase-locked loop (PLL) circuit mainly consists of a voltage-controlled oscillator(VCO), phase detector(PD) and low pass filter circuits(LPF). [3] The synchronisation of control signal is obtained by VCO ,which is installed in the feedback path. Oscillation frequency of VCO is denoted as  $f_{osc}$  and it is proportional to input supply voltage frequency( $f_i$ ). Output voltage frequency( $f_{osc}$ ) is proportional to the input voltage frequency( $f_i$ ) of VCO, and thus in closed loop circuit frequency of input supply voltage and the frequency of VCO output voltage is same i.e.  $f_{osc} = f_i$ . Fig 6 represents Block schematic diagram and circuit connection of analog phase lock loop circuit. Figure 7 represents complete hardware of PLL circuit. [8] This whole circuit is used to synchronize line frequency sine wave signal with PWM signal. For example, if line frequency is 49.8 Hz instead of 50 Hz, this circuit will automatically adjust its feedback to get the desired frequency. So in this way switching frequency is obtained as the multiple of the line frequency. Table-1 represents the components required for designing analog PLL circuit



**Fig 6: Block Schematic Diagram and Circuit Connection of Analog Phase Lock Loop Circuit**

| Sr No. | Description of block          | Components         |
|--------|-------------------------------|--------------------|
| 1      | Voltage Controlled Oscillator | IC 4046            |
| 2      | Multiplier IC                 | IC 4017            |
| 3      | Capacitors                    | 08uF, 1 UF         |
| 4      | Resistors                     | 1K,10K, 100K,6.8 K |
| 5      | 12 Volt Supply IC             | IC 7812            |

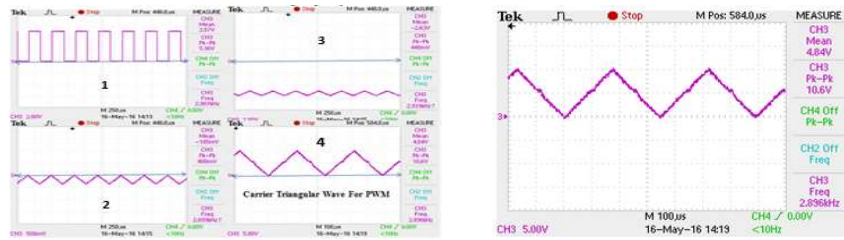
**Table 1: Components of PLL Hardware for Obtaining Line Synchronized Pulses.**



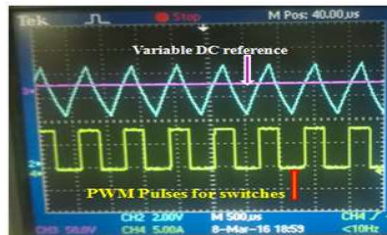
**Fig 7.a: Multiplier Circuit Using IC4017 b. Voltage Controlled Oscillator c. Complete Hardware Setup of PLL Circuit**

**PLL Hardware Results:**

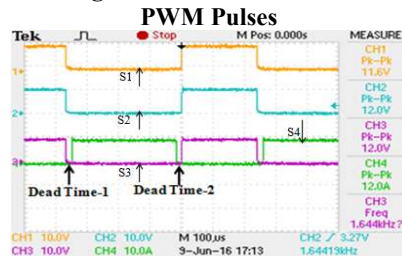
Figure 8 represents hardware results of PLL circuit which represents the waveform at different stages to obtain carrier triangular wave for PWM pulses. Fig 9(a) represents the hardware results of the methodology used for obtaining PWM pulses. With variable DC reference voltage, variable duty ratio can be obtained which in turn controls the speed of IM. Fig 9(b) represents PWM pulses for all four switches with dead band time -1 and time-2 between ON and OFF of the switches to avoid short circuit of series and freewheeling(parallel) switch at switching frequency of 2.86 kHz synchronized with the line frequency. Figure 10 represents line current and line voltage for phase A, indicating high power factor nearly equal to unity. Figure 11 represents graph of power factor v/s speed of IM for switching frequency of 2.86 kHz, which shows that pf is almost constant from lower speed to higher speed. Thus proposed topology works successfully with analog PLL technique.



**Fig 8: Carrier Triangular Wave from PLL, at 10.6 Volts, 2.86 kHz to Generate PWM Pulses**



**Fig 9 (a): Comparison of Carrier Triangular Wave with Variable DC Reference Voltage to Generate PWM Pulses**



**Fig 9 (b): PWM Pulses for All Four Switches, at 1.64 kHz Frequency Indicating Dead Band between Main Switch and Freewheeling Switch**



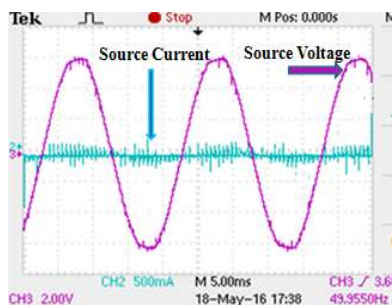


Fig 10: Motor Voltage and Motor Current of R-Phase at High Power Factor

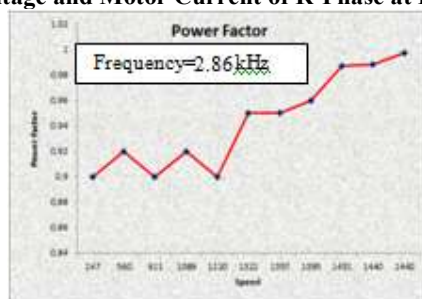


Fig 11: Graph of Speed Vs. Power Factor

### Conclusion

Thus, using PLL technique switching frequency of PWM pulses is multiple of supply frequency variable and thus got perfectly synchronized with the input supply frequency. Adding PWM and extinction angle pulse together and synchronizing it with the supply frequency separate control over wide range of speed from low to high and improvement in power factor near to unity is achieved. With This technique both control on speed and power factor of three phase induction motor, using only four semiconductor controllable switches, that contributes in simple control and cost effective converter has been achieved. With this technique IM runs at high power factor near to unity despite of speed of IM This has been realized with the novel features of the topology that, torque component of the input current increases and magnetizing component of current decreases, therefore overall current intake of the motor is reduced, which results in reduced power consumption. Since the magnetizing component of current is reduced stator copper loss ( $I^2R$ ) of the motor is also reduced, which in turn improves the efficiency of the motor.

### References

1. Bilal Saraçoğlu 4 May, 2010 "Supply power factor and load current harmonic performance improvement of three phase AC voltage Controller," Scientific Research and Essays, Vol. 5 (9),
2. Kushal Dhawad, R.D. Patane and Vittesh Naphade, February 2014. "Efficient Speed Control of 3-ph Induction Motor with Two Stage IPFC Using 1-ph Supply," International Journal of Emerging Science and Engineering (IJESE), Volume-2, Issue-4
3. N.V.Kuznetsov, G.A. Leonov, M.V. Yuldashev, R.V. Yuldashev Saint-2015 Simulation of the classical analog phase-locked loop based circuits Petersburg State University, Russia Dept. of Mathematical Information Technol. IFA papers online 48-1 (2015) 568-573
4. Somendra Banerjee, Dr. S. Chatterjee, Shimi. S. L, March 2014 "A Novel Four Switch Three Phase Inverter Controlled by Different Modulation Techniques – A Comparison", International Journal of Research in Electrical & Electronics Engineering, , vol. 2. Issue 1, pp. 14,23
5. Ahmed, N.A.; Mivatake. M.; Hyun Woo Lee; Nakaoka, M 2006." A Novel Circuit Topology of Three-Phase Direct AC -AC PWM Voltage Regulator", Industry Applications Conference., 41st IAS Annual Meeting. Conference Record of the 2006 IEEE, vol 4, no., pp.2076,2081
6. A dynamic phase error compensation technique for fast-locking phase-locked loops. IEEE journal of solid-state circuits, 2010
7. A fast and stable time locked loop for network time synchronization with parallel FLL and PLL 2018 IEEE international symposium on precision clock synchronization for measurement, control, and communication (ISPCS),
8. Date of Publication: 20 May 2015 An optimum loop gain tracking all-digital pll using autocorrelation of bang-bang phase-frequency Published in: IEEE Transactions on Circuits and Systems II: Express Briefs ( Volume: 62 , Issue: 9 , Page(s): 836 - 840 ISSN DOI: 10.1109/TCSII.2015.2435691

9. Date of Conference: 30 April-3 May 2017 Multi-Phase Sub-Sampling Fractional-N PLL With Soft Loop Switching For Fast Robust Locking Published in: 2017 IEEE Custom Integrated Circuits Conference (CICC) Date Added to IEEE *Xplore*: 27 July 2017 ISBN Information: Electronic ISSN: 2152-3630 INSPEC Accession Number: 17064056 DOI: 10.1109/CICC.2017.7993633 Publisher: IEEE
10. S.Y. Sun, Rockwell Int., Newport Beach, CA, US, Apr 1989 An analog PLL-based clock and data recovery circuit with high input jitter tolerance, Published in: IEEE Journal of Solid-State Circuits ( Volume: 24 , Page(s): 325 – 330, ISSN Information: INSPEC Accession Number: 3410004 DOI: 10.1109/4.18592 Publisher: IEEE